

CLAIMS

What is claimed is:

- 1 1. In a data processing system with a processor chip that includes a processor core, a store queue (STQ) mechanism with a store queue, and RC dispatch logic, a method for improving gathering capabilities for entries of the store queue that gather processor-issued store operations, said method comprising:
 - 5 gathering data of a first processor-issued store operation to an entry of the store queue;
 - 6 activating a timer to track elapsed time from a completion of the gathering step;
 - 7 when said timer reaches a pre-established threshold for elapsed time, signaling the arbitration logic that said entry is eligible for selection for dispatch to the RC dispatch logic; and
 - 9 when a second processor-issued store operation gathers to the entry before said pre-established threshold for elapsed time is reached:
 - 11 holding off tagging said entry as eligible for dispatch; and
 - 12 restarting said timer to track elapsed time from a completion of said gather of the second processor-issued store operation.
- 1 2. The method of Claim 1, further comprising:
 - 2 monitoring for a receipt of a barrier operation from said processor core; and
 - 3 when a barrier operation is received,
 - 4 tagging all active entries as eligible for dispatch; and
 - 5 preventing further gathering to said active entries, wherein a subsequent store operation targeting a cache line associated with one of said active entries is assigned a new entry within said store queue; and
 - 7 stopping a respective timer for each active entry.
- 1 3. The method of Claim 1, further comprising:
 - 2 tracking gathers to said entry to determine when said entry contains a full set of store operations to update an entire cache line;

4 when said contains a full set of store operations, signaling said entry as eligible for
5 dispatch independent of a current status of the timer for that entry, wherein a new gather to said
6 entry does not affect the entry's eligibility for dispatch.

1 4. The method of Claim 1, further comprising:
2 monitoring said entry to determining when said entry is still gatherable;
3 when said entry is no longer gatherable,
4 signaling said entry as eligible for dispatch; and
5 stopping said timer for the entry.

1 5. The method of Claim 4, wherein said timer is a counter that increments each clock tick of
2 a system clock within said data processing system and said threshold for elapsed time is a
3 saturation value of said counter, wherein said counter increment to saturation unless a new gather
4 occurs or said counter is stopped.

1 6. The method of Claim 5, wherein said STQ mechanism comprises a STQ controller and
2 said counter has an associated counter logic that activates, resets, and stops said counter, wherein
3 said counter logic further signals said STQ controller when said counter has reach said threshold
4 or is stopped.

1 7. A processor chip for utilization within a data processing system having a memory
2 hierarchy, said processor chip comprising:
3 a processor core;
4 a store queue having multiple entries, each having at least an address register and a data
5 register for storing address and data of a store operation issued by the processor core;
6 a store queue (STQ) controller having an associated arbitration logic, wherein said STQ
7 controller monitors said store queue and identifies when an entry is eligible to be selected for
8 dispatch by the arbitration logic; and
9 a plurality of timers and an associated timer logic, said plurality of timers being each
10 assigned to an entry and utilized for tracking elapsed time since a last gather of a store operation
11 to that entry; and

12 logic for signaling an entry as eligible to be selected for dispatch when the timer
13 associated with that entry reaches a pre-established threshold before another store operation
14 gathers into the entry.

1 8. The processor chip of claim 7, further comprising:
2 logic for gathering data of a first processor-issued store operation to the entry;
3 logic for activating the timer to track elapsed time from a completion of the gather of the
4 first processor-issued store operation;
5 when a second processor-issued store operation gathers to the entry before said pre-
6 established threshold for elapsed time is reached:
7 logic for holding off tagging said entry as eligible for dispatch; and
8 logic for restarting said timer to track elapsed time from a completion of said
9 gather of the second processor-issued store operation.

1 9. The processor chip of Claim 7, further comprising:
2 logic for monitoring for a receipt of a barrier operation from said processor core; and
3 when a barrier operation is received,
4 logic for tagging all active entries as eligible for dispatch; and
5 logic for preventing further gathering to said active entries, wherein a subsequent
6 store operation targeting a cache line associated with one of said active entries is assigned
7 a new entry within said store queue; and
8 logic for stopping a respective timer for each active entry.

1 10. The processor chip of Claim 7, further comprising:
2 logic for tracking gathers to said entry to determine when said entry contains a full set of
3 store operations to update an entire cache line;
4 logic that, when said contains a full set of store operations, signals said entry as eligible
5 for dispatch independent of a current status of the timer for that entry, wherein a new gather to
6 said entry does not affect the entry's eligibility for dispatch.

1 11. The processor chip of Claim 7, further comprising:

2 logic for monitoring said entry to determining when said entry is still gatherable;
3 when said entry is no longer gatherable,
4 logic or signaling said entry as eligible for dispatch; and
5 logic stopping said timer for the entry.

1 12. The processor chip of Claim 7, wherein said timer is a counter that increments each clock
2 tick of a system clock within said data processing system and said threshold for elapsed time is a
3 saturation value of said counter, wherein said counter increments to saturation unless a new gather
4 occurs or said counter is stopped.

1 13. The processor chip of Claim 12, wherein said timer logic that activates, resets, and stops
2 said counter, wherein said timer logic further signals said STQ controller when said counter has
3 reached said threshold or is stopped.

1 14. The processor chip of Claim 7, further comprising logic that, when said timer reaches a
2 pre-established threshold for elapsed time, said logic signals the arbitration logic that said entry
3 is eligible for selection for dispatch to the RC dispatch logic.

1 15. A data processing system comprising:
2 a processor chip that includes:
3 a processor core;
4 a store queue having multiple entries, each having at least an address register and
5 a data register for storing address and data of a store operation issued by the processor
6 core;
7 a store queue (STQ) controller having an associated arbitration logic, wherein
8 said STQ controller monitors said store queue and identifies when an entry is eligible to
9 be selected for dispatch by the arbitration logic; and
10 a plurality of timers and an associated timer logic, said plurality of timers being
11 each assigned to an entry and utilized for tracking elapsed time since a last gather of a
12 store operation to that entry; and

13 logic for signaling an entry as eligible to be selected for dispatch when the timer
14 associated with that entry reaches a pre-established threshold before another store
15 operation gathers into the entry; and
16 a memory hierarchy coupled to said processor chip.

1 16. The data processing system of claim 15, wherein said processor chip further includes:
2 logic for gathering data of a first processor-issued store operation to the entry;
3 logic for activating the timer to track elapsed time from a completion of the gather of the
4 first processor-issued store operation;
5 when a second processor-issued store operation gathers to the entry before said pre-
6 established threshold for elapsed time is reached:
7 logic for holding off tagging said entry as eligible for dispatch; and
8 logic for restarting said timer to track elapsed time from a completion of said
9 gather of the second processor-issued store operation.

10 17. The data processing system of claim 15, wherein said processor chip further includes:
11 logic for monitoring for a receipt of a barrier operation from said processor core; and
12 when a barrier operation is received,
13 logic for tagging all active entries as eligible for dispatch; and
14 logic for preventing further gathering to said active entries, wherein a subsequent
15 store operation targeting a cache line associated with one of said active entries is assigned
16 a new entry within said store queue; and
17 logic for stopping a respective timer for each active entry.

1 18. The data processing system of claim 15, wherein said processor chip further includes:
2 logic for tracking gathers to said entry to determine when said entry contains a full set of
3 store operations to update an entire cache line;
4 logic that, when said entry contains a full set of store operations, signals said entry as eligible
5 for dispatch independent of a current status of the timer for that entry, wherein a new gather to
6 said entry does not affect the entry's eligibility for dispatch.

7 19. The data processing system of claim 15, wherein said processor chip further includes:
8 logic for monitoring said entry to determining when said entry is still gatherable;
9 when said entry is no longer gatherable,
10 logic or signaling said entry as eligible for dispatch; and
11 logic stopping said timer for the entry.

1 20. The data processing system of claim 15, wherein:
2 said timer is a counter that increments each clock tick of a system clock within said data
3 processing system and said threshold for elapsed time is a saturation value of said counter,
4 wherein said counter increment to saturation unless a new gather occurs or said counter is
5 stopped; and
6 said timer logic that activates, resets, and stops said counter, wherein said timer logic
7 further signals said STQ controller when said counter has reach said threshold or is stopped.